Reviewed by: Andrew Newman

Module Name:Tx/Rx FIFO

Jira Ticket:[CAN2-18]

**CAN Controller Requirements Checklist Rev.0**

1. Is requirements document written clearly and grammatically correct?

Yes [ ] No [x]

Comments: FIFO\_W\_01 change w\_en to i\_w\_en.

1. Does requirements document define all functions to be performed by the module?

Yes [ ] No [x]

Comments: Initialization is missing reqs for all of the outputs of the module.   
FIFO\_INIT\_01 define it as FIFO\_DEPTH parameter with default depth of 2 and allowed range of values as mentioned. Refer to the depth as FIFO\_DEPTH in later reqs.  
Define internal naming for read and write pointers, adjust FIFO\_W\_02 and FIFO\_R\_02 accordingly to accommodate pointer into the memory buffer suggested.

Define memory buffer as separate requirement in the INIT and define a name for it to be referenced in read and write groups.(ideally you would have something line int\_queue[w\_pointer] for FIFO\_W\_02 for example; much less up to interpretation)

1. Does requirements document include all inputs and outputs to the module along with their corresponding accuracy, range of values, frequency and format?

Yes [ ] No [x]

Comments:Missing definitions for o\_overflow, o\_underflow.

1. Is each requirement unique?

Yes [x] No [ ]

Comments:

1. Does requirements document comply with system requirements and traceability?

Yes [ ] No [x]

Comments: See 3.

1. Is terminology consistent with Requirements Standards?

Yes [x] No [ ]

Comments:

1. Is it possible to implement all requirements?

Yes [x] No [ ]

Comments:

1. Is each requirement testable or verifiable?

Yes [x] No [ ]

Comments: